IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A magnetic random access memory comprising:

a silicon substrate;

a transistor which has a gate electrode formed on the silicon substrate via a gate insulating film and diffusion layers formed in the silicon substrate, the gate electrode being formed of polysilicon containing deuterium atoms;

a first insulating film formed on the silicon substrate and the transistor;

a multilayered interconnection formed in the first insulating film; and

a magneto-resistive element formed above the first insulating film,

wherein at least some of dangling bonds in the silicon substrate are terminated by silicon-deuterium bonds.

Claim 2 (Original): The memory according to claim 1, wherein the silicon-deuterium bonds exist at least partially in an interface portion between the gate insulating film and the silicon substrate under the gate electrode, junction portions of the diffusion layers, and a channel portion.

Claim 3 (Original): The memory according to claim 1, wherein deuterium atoms exist in the first insulating film.

Claim 4 (Currently Amended): The memory according to claim 1, wherein ~~deuterium atoms exist in the gate electrode~~ silicon-hydrogen bonds exist in the dangling bonds, and a ratio of the silicon-deuterium bonds to the silicon-hydrogen bonds is high in the dangling bonds.

Claim 5 (Original): The memory according to claim 1, wherein deuterium atoms exist in the gate insulating film.

Claim 6 (Currently Amended): The memory according to claim 1, further comprising a second ~~insulting~~ insulating film which is formed on the silicon substrate, including upper surfaces of the diffusion layers, and upper and side surfaces of the gate electrode and contains deuterium atoms.

Claim 7 (Original): The memory according to claim 1, wherein the magneto-resistive element is electrically connected to the transistor through part of the multilayered interconnection, and the transistor is a data read switching element.

Claim 8 (Original): The memory according to claim 1, wherein the transistor is a transistor of a CMOS circuit.

Claims 9-20 (Canceled).

Claim 21 (New): A magnetic random access memory comprising:

a silicon substrate;

a transistor which has a gate electrode formed on the silicon substrate via a gate insulating film and diffusion layers formed in the silicon substrate;

a silicon nitride film containing deuterium atoms and formed on an upper surface and side surfaces of the gate electrode;

a first insulating film formed on the silicon substrate and the silicon nitride film;

a multilayered interconnection formed in the first insulating film; and

a magneto-resistive element formed above the first insulating film,

wherein at least some of dangling bonds in the silicon substrate are terminated by silicon-deuterium bonds.

Claim 22 (New): The memory according to claim 21, wherein the silicon-deuterium bonds exist at least partially in an interface portion between the gate insulating film and the silicon substrate under the gate electrode, junction portions of the diffusion layers, and a channel portion.

Claim 23 (New): The memory according to claim 21, wherein deuterium atoms exist in the first insulating film.

Claim 24 (New): The memory according to claim 21, wherein silicon-hydrogen bonds exist in the dangling bonds, and a ratio of the silicon-deuterium bonds to the silicon-hydrogen bonds is high in the dangling bonds.

Claim 25 (New): The memory according to claim 21, wherein deuterium atoms exist in the gate insulating film.

Claim 26 (New): The memory according to claim 21, further comprising a second insulting film which is formed on the silicon substrate, including upper surfaces of the diffusion layers, and upper and side surfaces of the gate electrode and which contains deuterium atoms.

Claim 27 (New): The memory according to claim 21, wherein the magneto-resistive element is electrically connected to the transistor through part of the multilayered interconnection, and the transistor is a data read switching element.

Claim 28 (New): The memory according to claim 21, wherein the transistor is a transistor of a CMOS circuit.